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## NOTICE OF ALLOWANCE AND FEE(S) DUE

25859 7590 03/24/2004  
WEI TE CHUNG  
FOXCONN INTERNATIONAL, INC.  
1650 MEMOREX DRIVE  
SANTA CLARA, CA 95050

EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	PAPER NUMBER
2827	
DATE MAILED: 03/24/2004	

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,356	02/13/2002	Eric Juntwait		8882

TITLE OF INVENTION: LAYOUT FOR NOISE REDUCTION ON A PRINTED CIRCUIT BOARD AND CONNECTORS USING IT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	06/24/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

### HOW TO REPLY TO THIS NOTICE:

#### I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.
- ☐ Applicant claims SMALL ENTITY status.  
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER:** Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

# **PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to: Mail**

**Mail Stop ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
(703) 746-4000**

**or Fax**

**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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## **Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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**TITLE OF INVENTION:** LAYOUT FOR NOISE REDUCTION ON A PRINTED CIRCUIT BOARD AND CONNECTORS USING IT

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nonprovisional

NO

\$1330

\$300

\$1630

06/24/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
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PATEL, ISHWARBHAI B

2827

174-261000

**1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).**

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

**2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.**

1 \_\_\_\_\_  
2 \_\_\_\_\_  
3 \_\_\_\_\_

**3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)**

**PLEASE NOTE:** Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☐ corporation or other private group entity ☐ government

**4a. The following fee(s) are enclosed:**

- ☐ Issue Fee  
☐ Publication Fee  
☐ Advance Order - # of Copies \_\_\_\_\_

**4b. Payment of Fee(s):**

- ☐ A check in the amount of the fee(s) is enclosed.  
☐ Payment by credit card. Form PTO-2038 is attached.  
☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

**NOTE:** The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.**

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**TRANSMIT THIS FORM WITH FEE(S)**



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EXAMINER
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PATEL, ISHWARBHAI B

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DATE MAILED: 03/24/2004

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 11 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 11 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

982

<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/075,356	JUNTWAIT ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Ishwar (I. B.) Patel	2827	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on February 20, 04 and interview summary.
2. ☒ The allowed claim(s) is/are 1,2,4-6,8-13,15,18,21 and 22.
3. ☒ The drawings filed on 20 February 2004 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
  1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |   |  |
|---|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892)  | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)                              |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                | 6. <input checked="" type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date <u>0403</u> . |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),<br>Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment                                      |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material          | 8. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance                                |
|   | 9. <input type="checkbox"/> Other _____.   |

### EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Wei Te Chung (Reg. 43,325) on March 15, 2004.

The application has been amended as follows:

Amend / add the claims as below:

Claim 1 (currently amended): A noise reduced printed circuit board assembly comprising:

a substrate having at least two insulated layers (11, 12) for mounting conductive material;

a first set of conductive footprints (2) being mounted on one of the insulated layers (11), each footprint of said first set being accessible from outside of the substrate and electrically connectable with a corresponding ~~conductor~~ terminals extending from a terminal module, the ~~conductors~~ terminals being paired as differential pairs (y) and including at least two unpaired ~~conductors~~ terminals, the first and second ~~conductors~~ terminals, being closely spaced from and cross talked with each other; and

a second set of conductive footprints, at least one of the second set of conductive footprints (R3') being located on an area of the other insulated layers aligned with and spaced from one footprint (T2) of the first set and connected to another footprint (R3) of the first set; wherein

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said one footprint (T2) of the first set is connected with the first ~~conductor~~ terminal, and said another footprint (R3) of the first set is connected with a third ~~conductor~~ terminal which is of same differential pair with the second ~~conductor~~ terminal;

a plurality of connecting conductive traces (5) each being electrically connected to one footprint, the traces connected respectively to the footprints of every pair and being located on two different insulated layers; wherein

said traces located on two different insulated layers are aligned with each other along a predetermined distance.

Claim 2 (currently amended): The printed circuit board assembly as recited in claim 1, wherein at least two conductive footprints of the second set are located on different insulated layers.

Claim 4 (currently amended): The printed circuit board assembly as recited in claim[[3]] 1, wherein footprints of the first set are totally vertically aligned with their corresponding aligned footprints of the second set.

Claim 5 (currently amended): The printed circuit board assembly as recited in claim 1, wherein each footprint of the second set has the same size as its corresponding aligned footprint of the first set.

Claim 6 (currently amended): The printed circuit board assembly as recited in claim 5, wherein each footprint of the second set is totally vertically aligned with its corresponding aligned footprint of the first set.

Claim 8 (currently amended): The printed circuit board assembly as recited in claim 1, wherein every footprint of the second set has an expanding size larger than its corresponding aligned footprint of the first set.

Claim 9 (currently amended): The printed circuit ~~bare~~ board assembly as recited in claim 1, wherein each footprint of the first set is a solderably conductive pad.

Claim 10 (currently amended): The printed circuit board assembly as recited in claim 1, wherein the printed circuit board is a built-in circuit board of a connector and all the necessary electronic components of the connector including conditioning ~~component~~ components and said terminal module are solderable on the printed circuit board.

Claim 11 (currently amended): A layout of a printed circuit board assembly for noise reduction comprising:

a plurality of footprints (2) being mounting on an outer face of a substrate of the printed circuit board, every footprint being electrically connected with a corresponding ~~conductor~~ terminal from ~~an electrical device~~ a terminal module, every two of the ~~conductors~~ terminals being a signal based pair;

a plurality of connecting conductive traces (5) each being electrically connected to one footprint, portions of every trace extending along at least one intermediate layer located in the substrate of the printed circuit board for easiness to be electrically connected to other functional circuit of the printed circuit board; wherein

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each trace connected to a first ~~chosen~~ pair of footprints (T3, R3) is relocated to have portion of them pass through an area of the intermediate layer vertically spaced from the location of one footprint of a second ~~chosen~~ pair (R2, T2) on the outer face of the substrate and an expanded conductive footprint (T3', R3') is formed over there to couple with the footprint it faces; wherein

said traces located on two different insulated layers are aligned with each other along a predetermined distance.

Claim 12 (currently amended): The layout of the printed circuit board assembly as recited in claim 11, wherein the expanded conductive footprint

connected to one footprint of the first ~~chosen~~ pair is coupled with the footprint of the second ~~chosen~~ pair which bears a coupled signal from the ~~electrical device terminal module~~ when the ~~conductor terminal~~ connected to said footprint of the second ~~chosen~~ pair is coupled with the ~~conductor terminal~~ connected to the other footprint of the first ~~chosen~~ pair before the signals are transferred to the corresponding footprints.

Claim 13 (currently amended): The layout of the printed circuit board assembly as recited in claim 11, wherein at least one expanding conductive footprints has the same size as its coupling footprint mounted on the outer face.

Claim 15 (currently amended): The layout of the printed circuit board assembly as recited in claim 11, wherein the substrate has at least two different intermediate layers and at least one conductive trace portion extends along every intermediate layer.

Claim 17 (canceled)



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Claim 18 (currently amended): A printed circuit board assembly comprising:

a substrate (10) having at least two insulated layers (11, 12);

a plurality of footprints (2) being mounting on one insulated layer of the substrate of the printed circuit board, every footprint being electrically connected with a corresponding ~~conductor~~ terminal ~~from an electrical device a~~ terminal module, every two of said ~~conductors~~ terminals being a signal based

pair;

a plurality of connecting conductive traces (5) each being electrically connected to one footprint, the traces connected respectively to every footprint of one ~~chosen~~ pair and being located on two different insulated layers; wherein

said traces located on two different insulated layers are aligned with each other along a predetermined distance.

Claims 19 and 20 (canceled)

Claim 21 (new): The printed circuit board assembly as recited in claim 18, said substrate (10) defining at least three mounting surfaces (11, 12, 13), there being first, second and third conductive traces, the first trace including first, second and third sections (T3, T3', C3), the second conductive trace including first, second and third traces (R2, R2', C2'), the third conductive trace including first, second and third traces (R3, R3', C3'), wherein said sections (T3, T3', R2, R2', R3, R3') are essentially the footprints; wherein the first sections (T3, R2, R3) of the first, second and third conductive traces are all arranged in the common mounting surface (11); wherein the second section (T3') of the first conductive trace is arranged in the second mounting surface (12) and is aligned with the first section (R2) of the second conductive trace; wherein the third section (C3) of the first conductive trace is aligned with the third section (C3') of the third conductive trace.

Claim 22 (new): The printed circuit board assembly as recited in claim 18, said substrate defining first, second and third layers stacked upon one another, first, second, third and fourth footprints (T2, T3, R3, R2) side by side located on the first layer in sequence wherein said first footprint and said fourth footprint are differential pair, and said second footprint and said third footprint are another differential pair, a fifth footprint (R3') located on the second layer, and

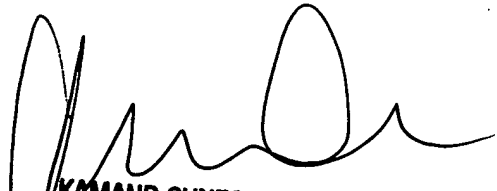
vertically aligned with the first footprint (T2) and electrically connected to the third footprint (R3) for somewhat counterbalancing crosstalk between the first footprint (T2) and the second footprint (T3) generated around the first layer, and a sixth footprint (T3') located on the third layer, and vertically aligned with the fourth footprint (R2) and electrically connected to the second footprint (T3) for somewhat counterbalancing crosstalk between the third footprint (R3) and the fourth footprint (R2) generated around the first layer; wherein a distance between the first layer and the second layer is different from the first layer and the third layer, and a size of said fifth trace (R3') and that of said sixth trace (T3') are dimensioned according to those distance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ibp  
March 15, 2004



**KAMAND CUNEO**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**